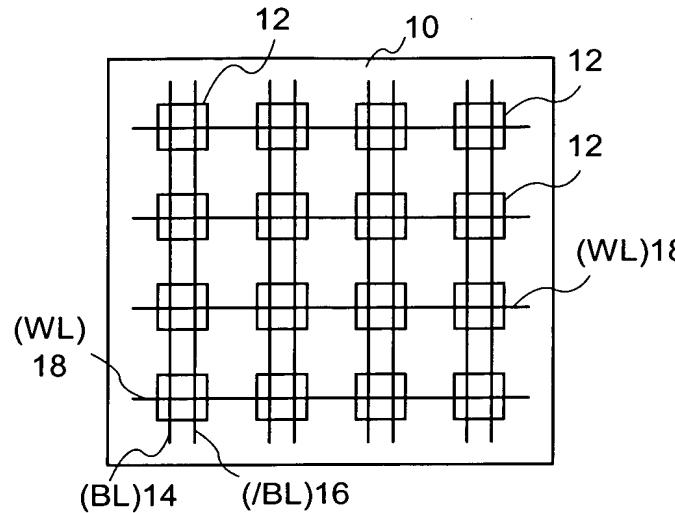


Replacement Sheet

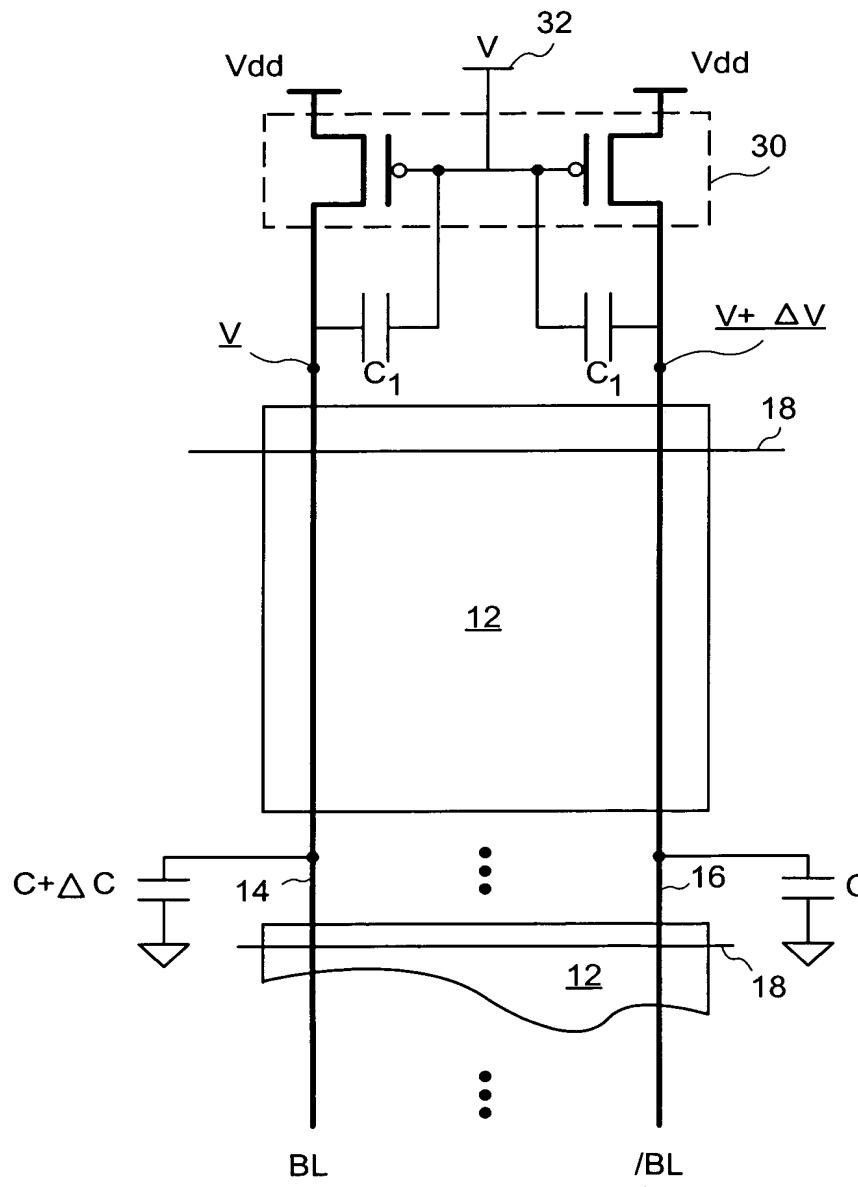
Title: MEMORIES HAVING REDUCED BITLINE VOLTAGE OFFSETS

Inventors: Scott T. Becker

Docket No: ARTCP012C App No: 10/026,245



**FIG. 1A**  
(prior art)



**FIG. 1B**  
(prior art)

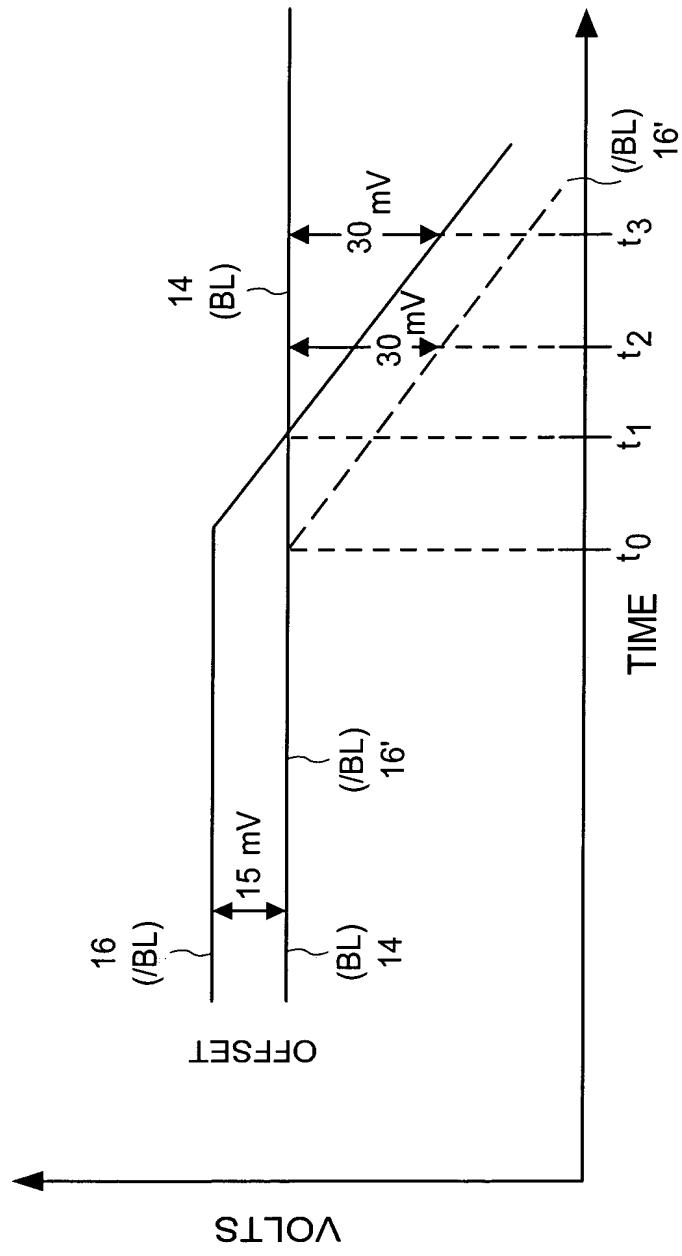


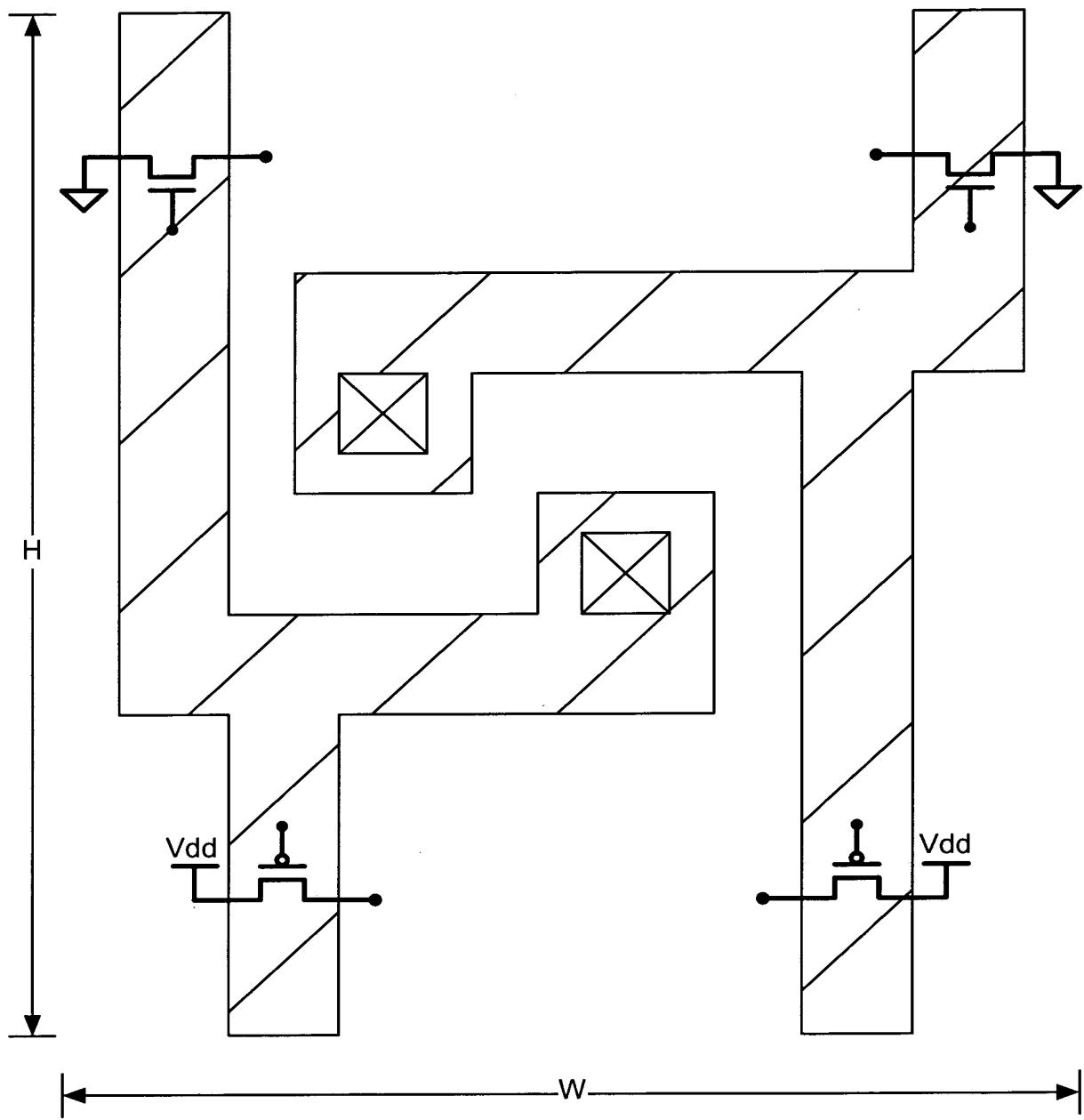
FIG. 1C  
(Prior Art)

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**FIG. 1D**  
(prior art)

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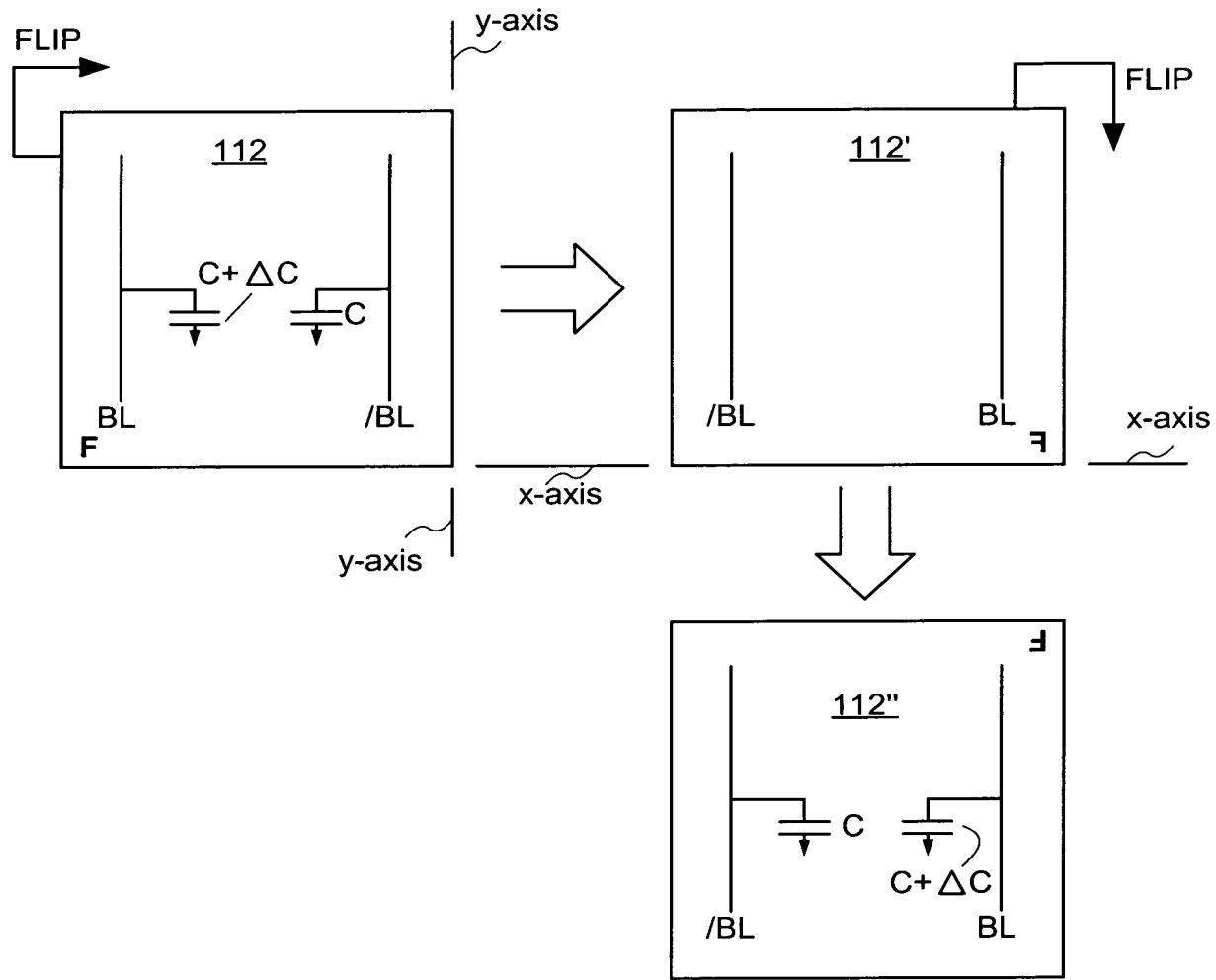


FIG. 2A

Replacement Sheet

Title: MEMORIES HAVING REDUCED BITLINE VOLTAGE OFFSETS

Inventors: Scott T. Becker

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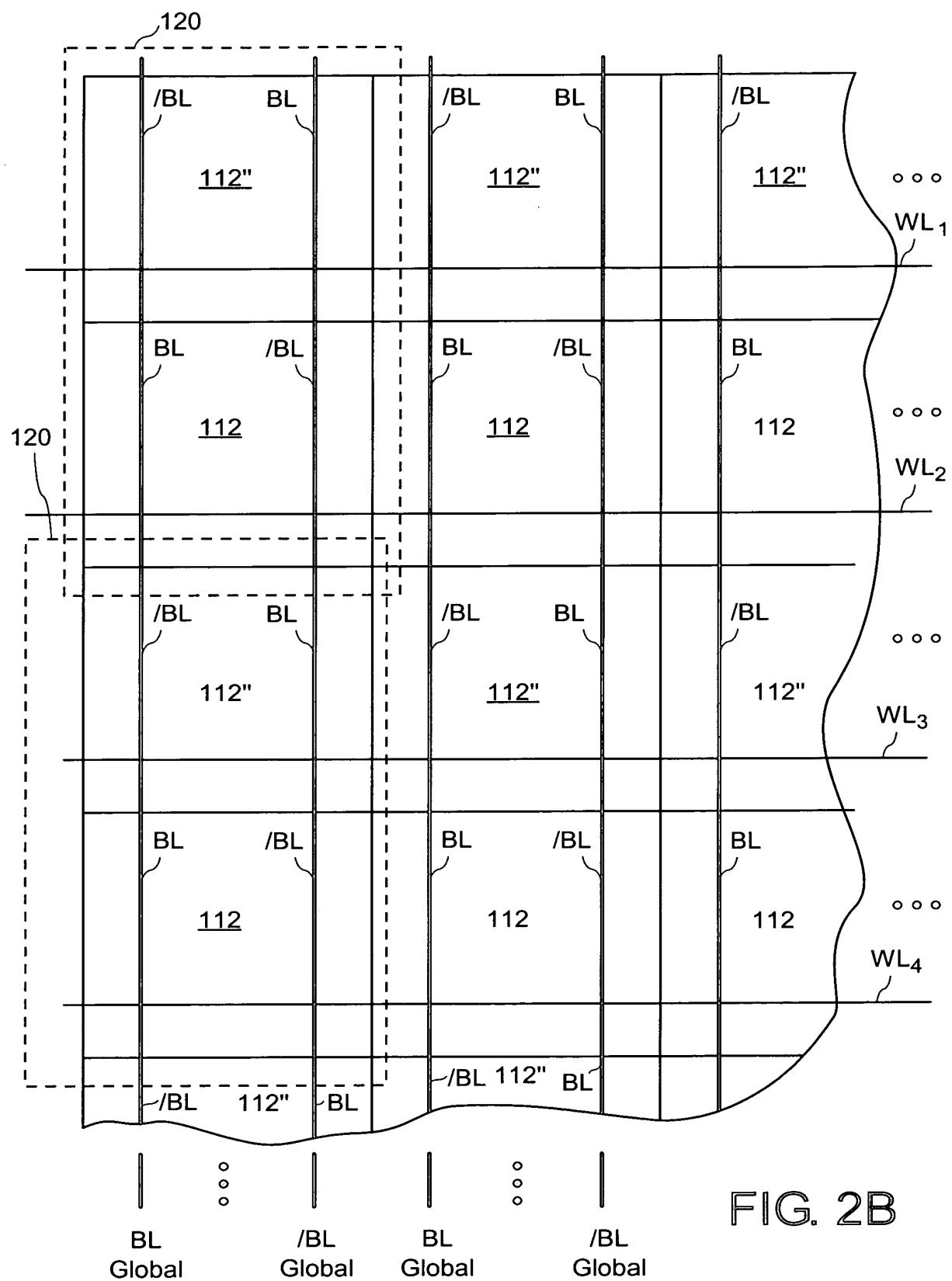


FIG. 2B

Replacement Sheet

Title: MEMORIES HAVING REDUCED BITLINE VOLTAGE OFFSETS

Inventors: Scott T. Becker

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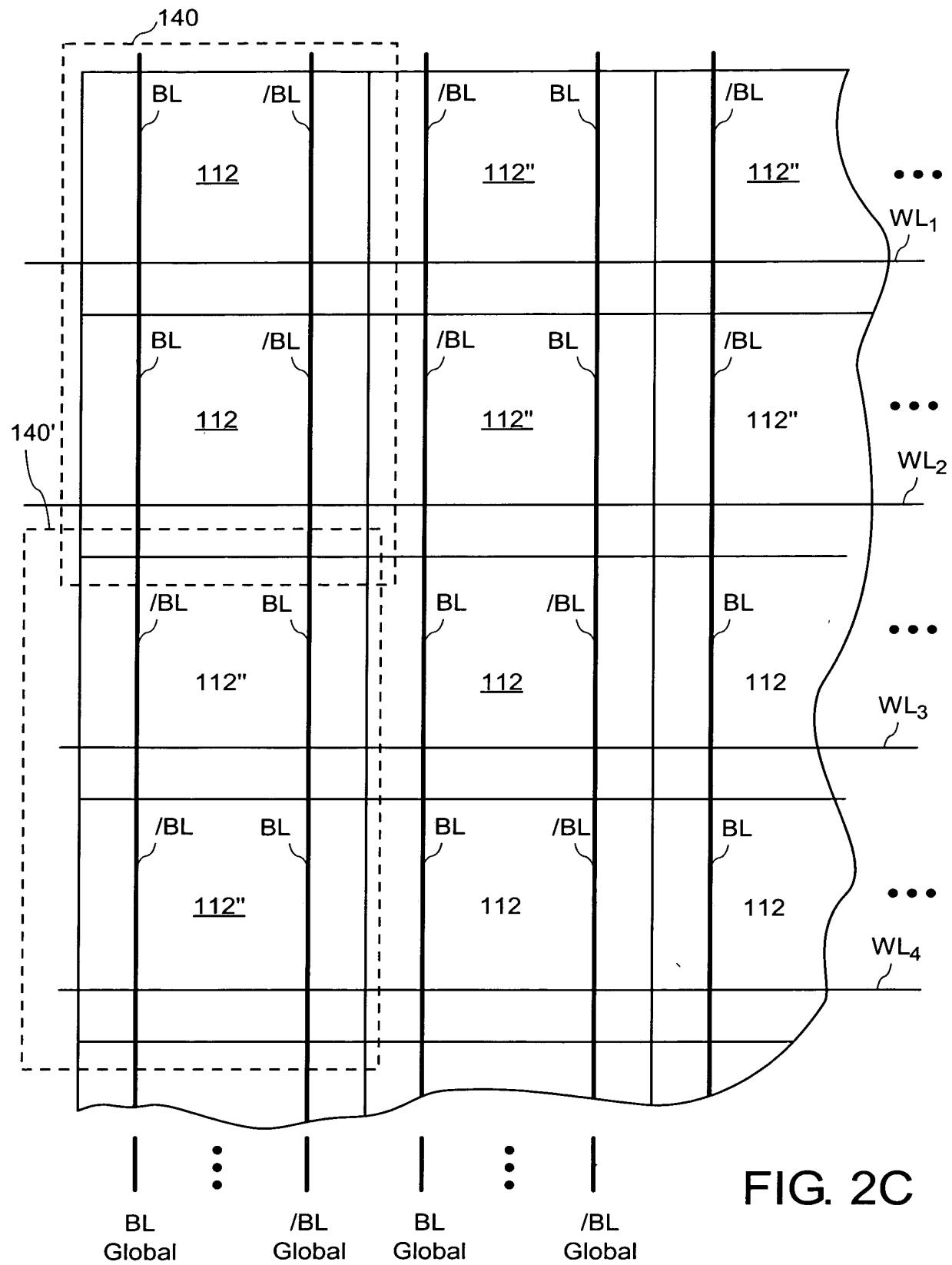


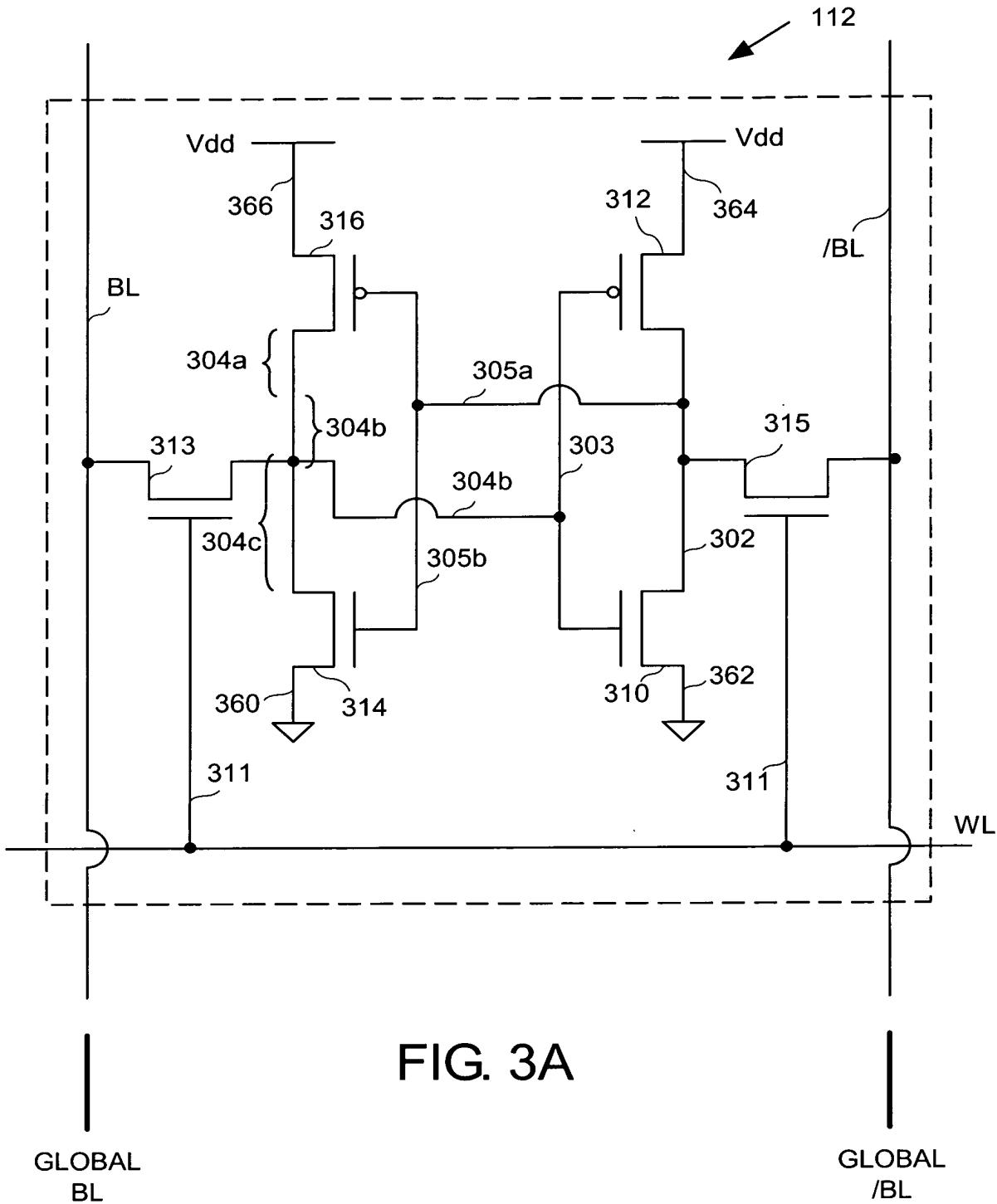
FIG. 2C

Replacement Sheet

Title: MEMORIES HAVING REDUCED BITLINE VOLTAGE OFFSETS

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Replacement Sheet

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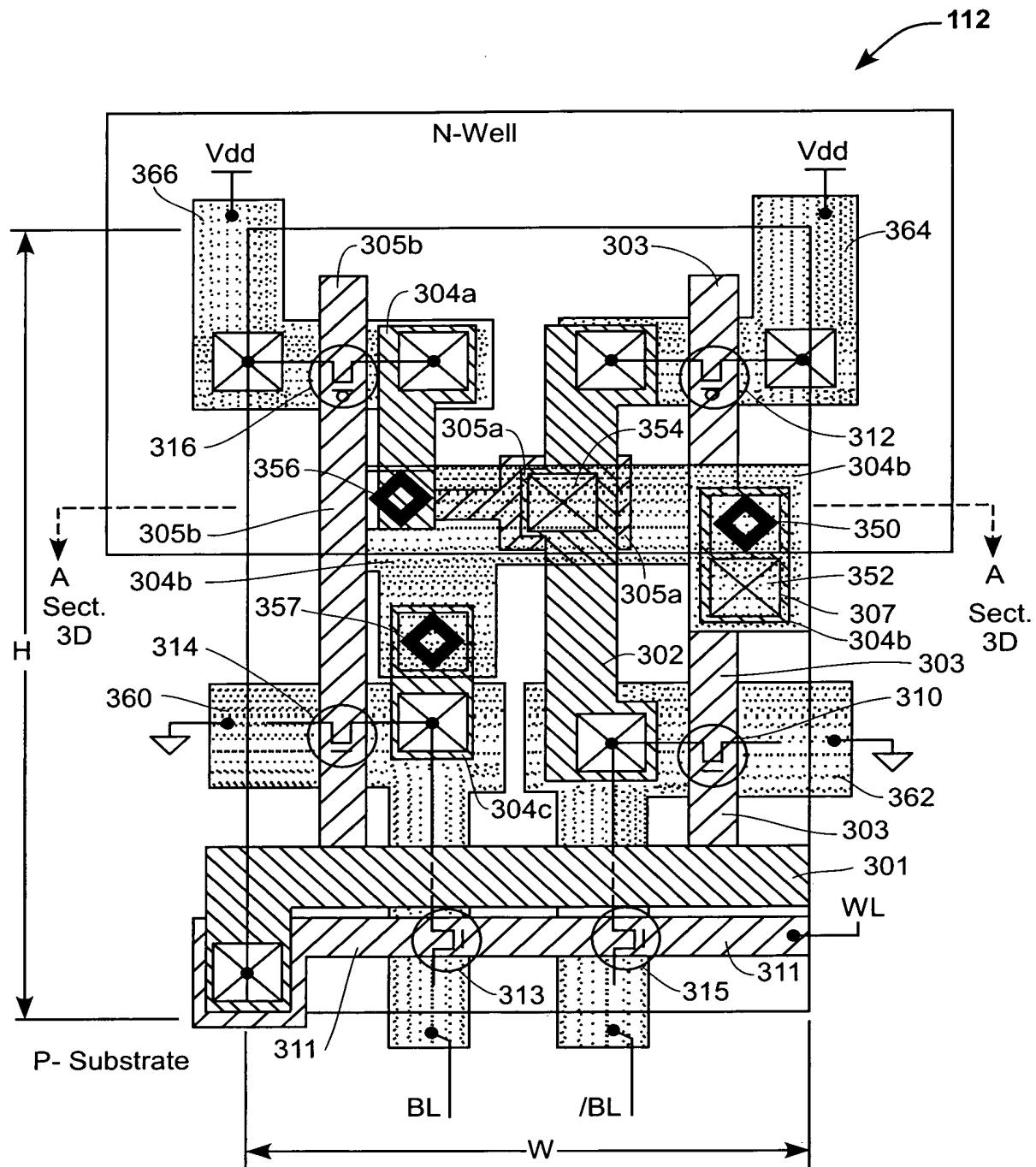


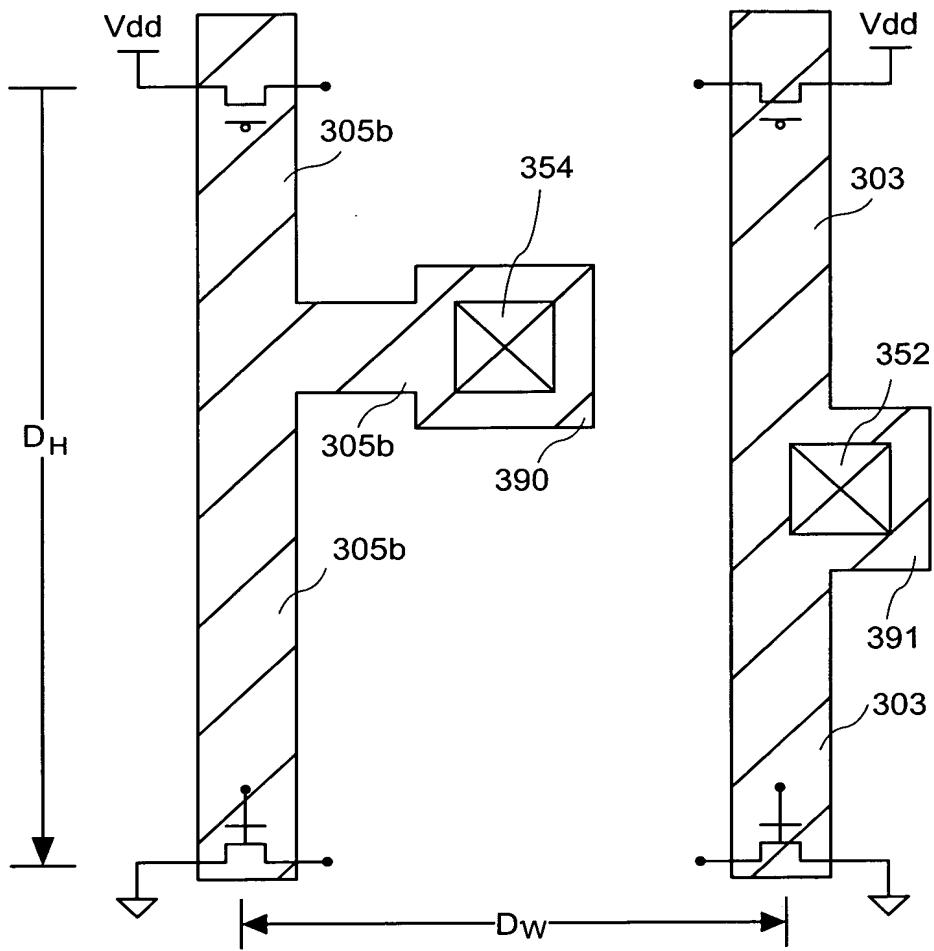
FIG. 3B

Replacement Sheet

Title: MEMORIES HAVING REDUCED BITLINE VOLTAGE OFFSETS

Inventors: Scott T. Becker

Docket No: ARTCP012C App No: 10/026,245



**FIG. 3C**

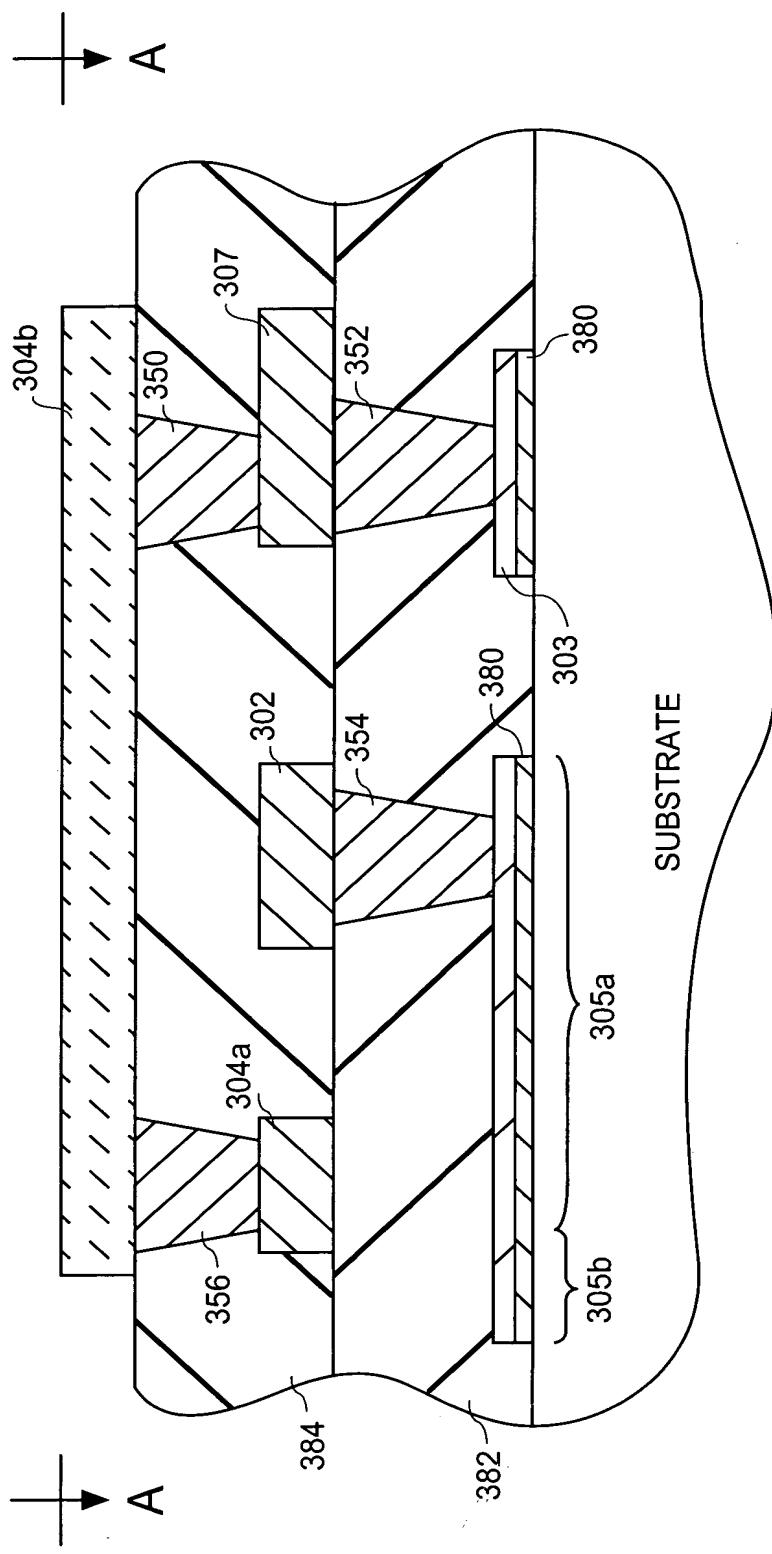


FIG. 3D